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FPGA SYSTEM ERROR RATE ANALYSIS FOR HARSH RADIATION ENVIRONMENTS



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Outline

- Introduction
- Background
 - FPGA Radiation Effects
 - Mitigating FPGA Radiation Effects
 - Harsh Radiation Environments
- Test Methodology
 - Fault Injection
 - Proton Accelerator
- - Fault Injection
 - Proton Accelerator
- SEU Rate Models
- Estimating Probability of Failure





Introduction

FPGA computation capabilities

- FPGAs are well-suited to remote-sensing, comms and other DSP applications often used in space
- Large percentage of FPGA space applications target LEO
 - LANL CFE, NASA GRACE, U. Southern Australia FedSat, NASA TACSAT-2, etc.
- We want to extend the reach of FPGAs to more interesting orbits
 - e.g. GPS, GEO, Molniya, Polar, etc.





Background :: FPGA Radiation Effects

- □ Single Event Upsets (SEU)
 - Change of state in memory structure
 - A significant portion of SRAM-based FPGA memory cells are dedicated to the user's circuit design (configuration memory)
 - SEUs in the configuration memory can modify the actual operation of the circuit
- Mitigating FPGA Radiation Effects
 - Triple modular redundancy (TMR)
 - XTMR style of TMR with triplicated voters must be employed to eliminate all single points of failure
 - Scrubbing
 - Periodic or continuous refresh of configuration memory back to intended state
 - Prevents accumulation of upsets in configuration memory
 - Reduces probability of simultaneous upsets (i.e. multiple independent upsets, MIUs) in configuration memory





Background :: Mitigating FPGA Radiation Effects (cont.)

Multiple independent upsets (MIUs) can defeat TMR and scrubbing



Background :: Harsh Radiation Environments

- Solar energetic particle (SEP) events (colloquially known as solar flares)
 - Harshest radiation environment in space Earth orbits (Tylka et al.)
 - SEU rate can increase orders of magnitude
 - Modeled in CREME96 by week-long event in October 1989
 - Primarily affect orbits further away from the Earth's magnetic field or at the poles (e.g. GPS, GEO, Molniya, Polar)
- □ An increase in SEU rate increases the likelihood of MIUs
- The purpose of this work was to measure the probability of failure from MIUs during SEP events





Testing Methodology :: Fault Injection



Algorithm

do {

- generate `i' random bits to upset
- inject `i' upsets into bitstream
- check for output error
- fix upset bits
- reset device
- record data to output file
- } while trials < `m'</pre>



Testing Methodology :: Accelerator

- $\Box \quad DUT = Xilinx Virtex-4 XC4VSX55$
- Crocker Nuclear Laboratory, UC Davis
- 63 MeV Protons



BYU BYU BYU BYU

- Algorithm
- do {
 - sleep for time 't'
 - get and fix upset frames
 - if upsets found
 - record upsets to file
 - check for output error
 - reset DUT
- } while time < `T'</pre>



Results :: Example Circuits

- BYU Shift Reg
 - 32-bit wide, 250 stage shift register with arbitrary combinational logic between each stage
- □ Shift Reg 1b
 - 1-bit wide, 16,200 stage shift register

□ SSRA

 Digital signal processing kernel

Design	Design Utilization - Slices		
	No TMR	TMR	
BYU Shift Reg	4011 (16%)	12014 (48%)	
Shift Reg 1 b	8111 (33%)	24314 (98%)	
SSRA	5381 (21%)	18591 (75%)	



Results :: Fault Injection

10



Note: A minimum of 1000 events were observed for each data point.





Results :: Fault Injection







Results :: Accelerator

12



Note: A minimum of 30 events were observed for each data point.





SEU Rate Models

Orbit	Apogee (km)	Perigee (km)	Inclination (deg)	Peak 5-Minute SEU Rate (SEUs/Device/s)
GEO	35786	35786	0	3.29E-1
GPS	20200	20200	55	2.85E-1
Molniya	39305	1507	63.2	3.08E-1
Polar	833	833	98.7	7.84E-2

- SEU Rate Models
 - CREME96: Worst Week, Worst Day, Peak 5-minutes (see data above)
 - What actually happens during that peak 5-minutes?
 - Real Answer: Nobody Knows!!
 - But we can bound the problem...
 - Best Case: Fluence is perfectly averaged over 5 minutes

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Worst Case: Fluence all comes during one scrub cycle



Estimating Probability of Failure

- Goal: Estimate probability of failure P(F_{5-min}) for the CREME96 peak 5 minutes
 - Requires probability of i upsets per scrub cycle P(A_i)
 - Requires conditional probability of failure for a particular scrub cycle given i upsets occurred during that particular scrub cycle P(F_{1-cycle} | A_i)
 - **Requires probability of failure P(F_{1-cycle}) for one trial (i.e. one scrub cycle)**
- \Box We measured P(F_{1-cycle} | A_i) using fault injection and the accelerator
- □ We assume that P(A_i) has a Poisson probability density function (pdf) since n >> 1 and t_a << T; with parameter $\lambda = (t_a * n)/T$, i.e. $\lambda =$ the SEU rate
 - \Box T = interval, e.g. 5 minutes
 - n = number of upsets, e.g. 100 upsets in peak 5 minutes
 - \bullet t_a = length of sub-interval, e.g. 15 millisecond scrub cycle
- \Box We calculate P(F_{1-cycle}) for one scrub cycle using the following equation

$$P(F_{1-\text{cycle}}) = \sum_{i=0}^{\infty} P(F_{1-\text{cycle}} \mid A_i) P(A_i)$$





Estimating Probability of Failure

- 15
- If we assume that each scrub cycle is an independent trial (valid if scrubbing works correctly), then we can use the following fundamental theorem from Bernoulli to compute P(F_{5-min}) over the entire 5 minute interval

$$P(F_{5-\min}) = \sum_{i=1}^{m} {m \choose i} P(F_{1-cycle})^{i} (1 - P(F_{1-cycle}))^{m-i}$$

or
$$P(F_{5-\min}) = 1 - \sum_{i=0}^{0} {m \choose i} P(F_{1-cycle})^{0} (1 - P(F_{1-cycle}))^{m-0}$$

$$= 1 - (1 - P(F_{1-cycle}))^{m}$$

m = number of trials (assuming 15 millisecond scrub cycle, m=20,000 in five minutes)





Estimating Probability of Failure :: Example (SSRA TMR design, GEO orbit, CREME96 "Best Case" model)



$$P(F_{1-cycle}) = \sum_{i=0}^{\infty} P(F_{1-cycle} | A_i) P(A_i)$$

= 9.7 x10⁻⁸
$$P(F_{5-min}) = 1 - (1 - P(F_{1-cycle}))^m$$

= 1 - (1 - 9.7 x10⁻⁸)²⁰⁰⁰⁰
= 1.9 x10⁻³





Estimating Probability of Failure :: P(F) Estimates

17



Conclusion

- Multiple independent upsets (MIUs) can defeat TMR and scrubbing
- SEP events can cause MIUs, particularly in strategic orbits with little or no protection provided by the Earth's magnetic field
- An example circuit's response to various sizes of MIUs was measured using fault injection and verified at a proton accelerator
- Probability of failure can be estimated using CREME96 SEU rates and MIU response data (fault injection or accelerator), however CREME96 SEU rate data are insufficient to make high fidelity estimates
 - We tried creating a model based on an extrapolation from the CREME96 worst week, worst day and peak 5 minutes, but p(F_{5-min}) was approximately the same as the "best case" model
 - Better models are needed
- Probability of failure estimates for an example circuit were presented
 - P(F) = 1.99E-3 in the best case
 - P(F) = .987 in the worst case





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BACKUP SLIDES



Background :: Single Event Effects

□ Single Event Upsets (SEU)

Change of state in memory structure







Background :: FPGA Radiation Effects

- A significant portion of SRAM-based FPGA memory cells are dedicated to user's circuit design (configuration memory)
- Upsets in the configuration memory can modify the actual operation of the circuit





Background :: Mitigating FPGA Radiation Effects

Triple Modular Redundancy





22

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- EST 1843

Background :: Mitigating FPGA Radiation Effects

Scrubbing

- Periodic or continuous refresh of configuration memory back to intended state
- Prevents accumulation of upsets in configuration memory
- Reduces probability of simultaneous multiple independent upsets (MIUs) in configuration memory





Results :: Accelerator

24







Results :: Accelerator

25







SEU Rate Models :: Logarithmic Fit SEU Rate Model

